DIMMABLE COLD-CATHODE FLUORESCENT LAMP BALLAST DESIGN USING THE UC3871

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ABSTRACT

This application note describes how to design a resonant cold-cathode fluorescent lamp converter and liquid crystal display (LCD) bias supply using the UC3871. A design method is presented and an example circuit is designed. Practical considerations regarding component selection and layout are discussed, and performance results are shown.

DESIGN CONSIDERATIONS

The UC3871 provides a complete power supply control solution for backlit LCDs that are typically used in laptop and notebook computers, and portable instrumentation. These applications require an adjustable high voltage AC current source to drive a cold cathode fluorescent lamp (CCFL) and an adjustable low voltage DC supply to bias the LCD. The UC3871 provides all control functions for these two supplies and also incorporates protection and synchronization circuitry. A low power shut-down input places the entire circuit into a very low current standby mode to reduce battery drain in portable systems and eliminate the need for a low-drop series switch.

The power circuitry illustrated in figure 1 consists of three sections:

1. A pulse width modulated (PWM) buck regulator to provide a variable, regulated voltage
2. A zero voltage switched (ZVS) resonant push-pull converter to transform the variable, regulated voltage to a high voltage AC output
3. A PWM flyback regulator to generate a variable DC voltage to bias an LCD

The buck and flyback regulators are synchronized to the ZVS push-pull converter, which free runs at its resonant frequency. Unitrode application note U-141 also covers the UC3871, along with further description and analysis of this topology and the application's requirements.

Most potential applications for the UC3871 are sensitive to both size and efficiency. EMI generation is also critical because only limited shielding is possible. The size/efficiency trade off is primarily in the magnetics, with the high voltage transformer by far the single most critical component. The design therefore must begin with an assessment of the performance and size goals, and their impact on the transformer design. In general, higher frequencies are preferred to minimize the size of the buck and flyback regulator magnetics, but excessively high frequencies will cause significant efficiency degradation.

DESIGN PROCEDURE

The ZVS resonant push-pull converter is designed first, and then the buck regulator and LCD bias flyback converter since both of these circuits are dependent on the push-pull converter. Resonant push-pull converter design requires an iterative approach because almost all of the variables are interdependent. A few initial variables come from the lamp and application specifications. These are normally the lamp starting voltage, operating voltage, and operating current, and the input supply voltage range. The desired resonant frequency is then chosen in order to calculate the remaining variables.

To help illustrate the design procedure, the following design example is presented which is typical of what a small computer would use for LCD power and back lighting. The application requirements are as follows:

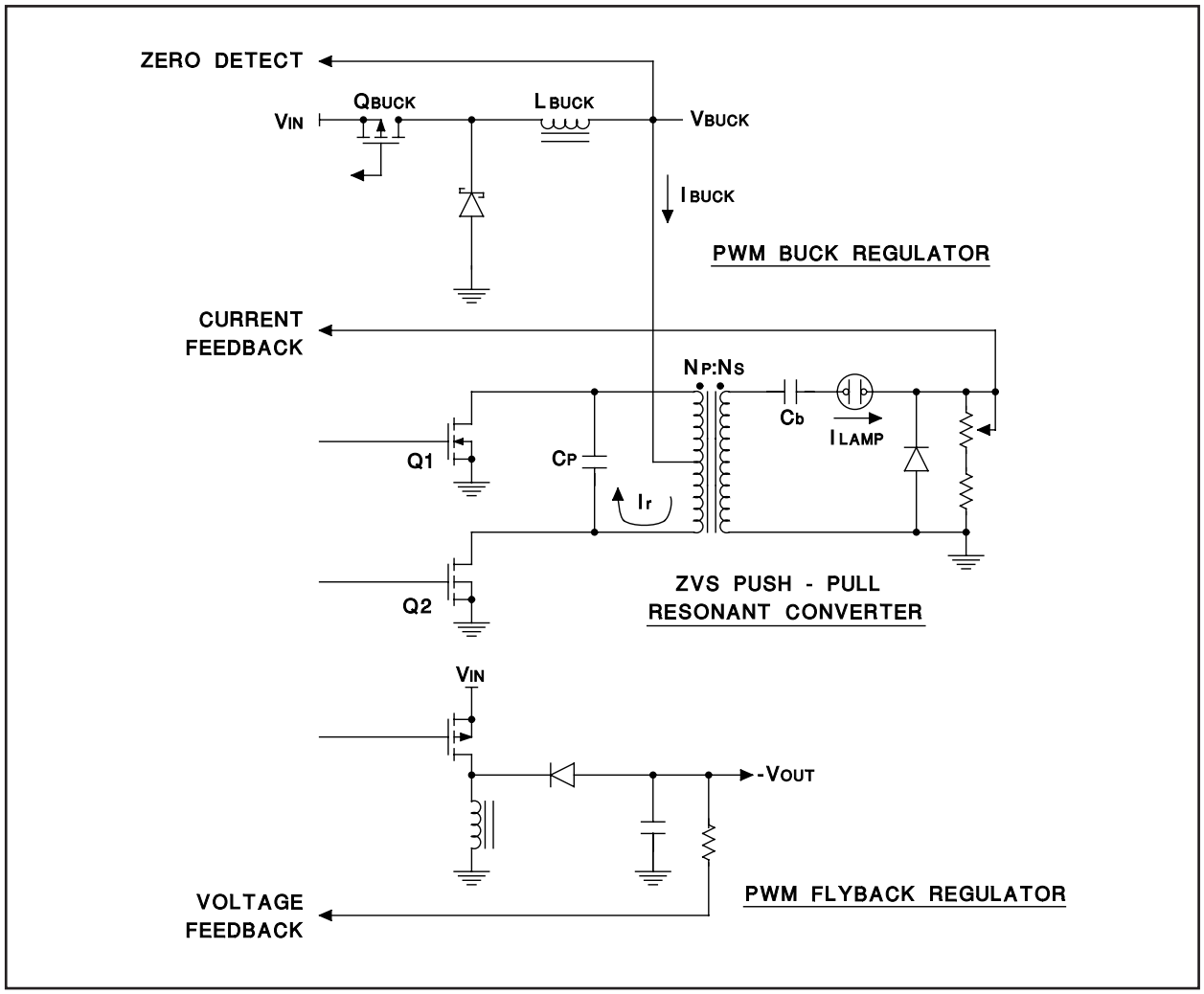

Figure 1. The power circuitry consists of three sections.

Input Voltage Range (Vin) 4.5V to 18V

LCD Bias Supply:

Output Voltage (Vlcd) -12V to -24V

Output Current (Ilcd) 25mA

Fluorescent Lamp Ballast:

Starting Voltage (Vlamp) 900V (peak)

Operating Voltage (Vlamp) 350V (peak)

Operating Current (Ilamp) 0.5mA to 5mA (avg.)

The desired minimum resonant frequency is 50kHz so that the buck and flyback operating frequency will be at least 100kHz. At this frequency, switching losses will be low. Increasing the frequency will allow smaller magnetics, but efficiency will most likely suffer. The complete schematic of the design example circuit is shown in figure 2.

ZVS RESONANT PUSH-PULL CONVERTER

The minimum input voltage and maximum lamp starting voltage determine the minimum transformer turns ratio. After calculating the initial transformer parameters, the turns ratio should be checked to make sure that full load current can be developed at the minimum input voltage. The minimum turns ratio is then:

$$\frac{N_S}{N_P} \geq \frac{V_{START(PEAK)}}{\pi V_{INmin}} \quad (1)$$

$$\geq \frac{900}{4.5\pi}$$

$$\geq 64$$

Note that this ratio relates the entire primary winding to the secondary. Sometimes the turns ratio is specified to relate one-half of the primary winding (end to center-tap) to the secondary.

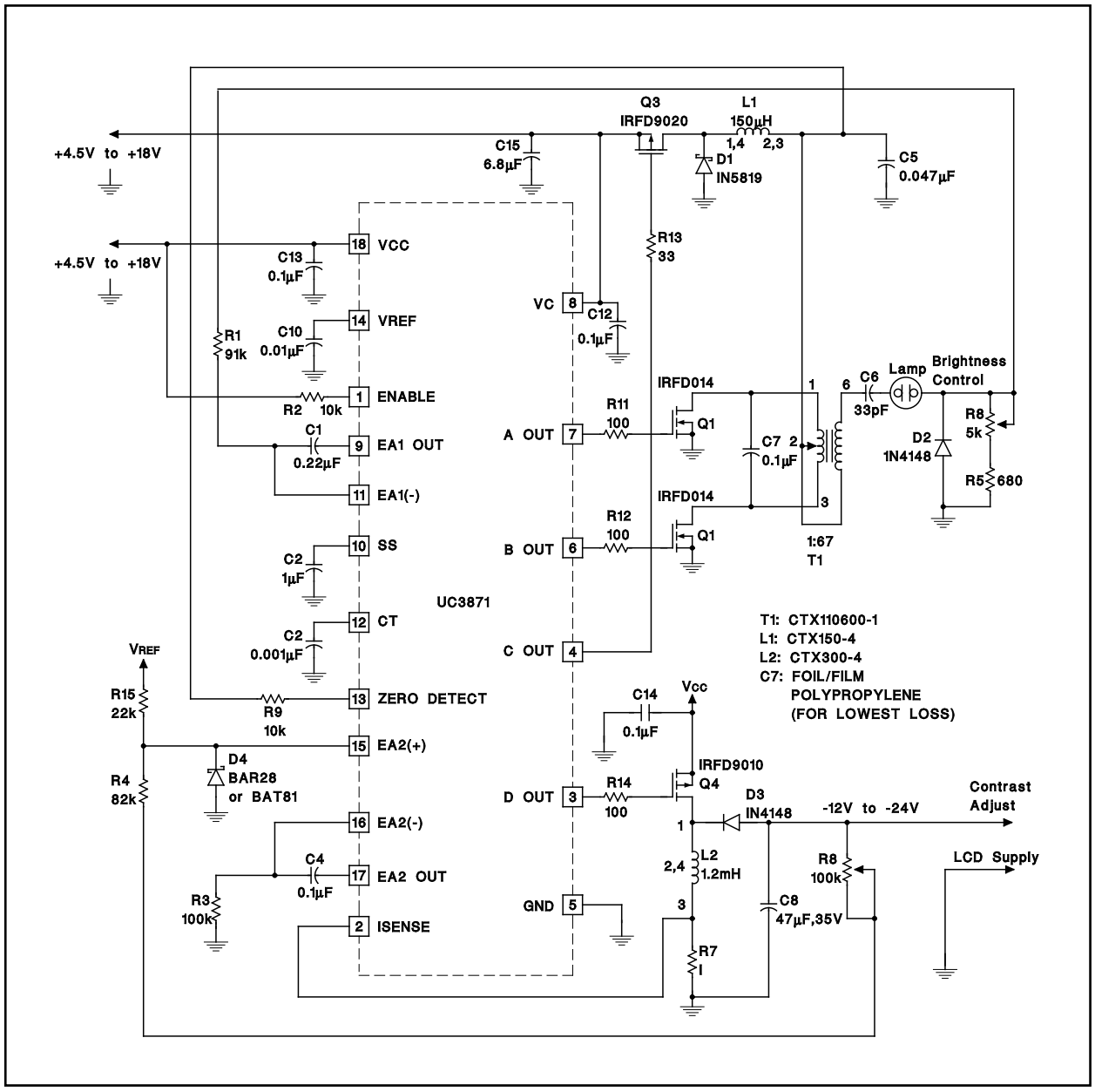

Figure 2. Complete circuit schematic.

A nominal ballast capacitor (Cb) value is calculated by setting the voltage across the ballast capacitor approximately twice the lamp sustaining voltage. This is an arbitrary relationship which serves as a starting point. Dropping a large voltage across the ballast capacitor voltage gives the converter a high output impedance and makes the converter relatively insensitive to the lamp's highly nonlinear impedance. Unfortunately, it also increases the circuit's losses. Tradeoffs between circuit size, distortion, and efficiency are governed by this component, so further iterations will usually result in a different final value. Setting the ballast capacitor's voltage equal to twice the lamp voltage at maximum current and minimum resonant frequency gives the value for Cb:

$$V_{CB} = \frac{I_{LAMP}}{2\pi F C_B} = 2V_{LAMP} \quad (2)$$

$$C_B = \frac{I_{LAMP}}{4\pi F V_{LAMP}}$$

$$= \frac{0.005}{4\pi(50 \cdot 10^3)(222)}$$

$$= 36pF$$

High secondary voltage and turns ratio result in poor coupling between the transformer's primary and secondary windings resulting in high leakage inductance. Capacitors across both the primary and secondary windings form two loosely coupled

parallel resonant circuits. To minimize output distortion, the independent primary and secondary resonant frequencies should be approximately the same. This requirement establishes a desired relationship between the primary (Cp) and secondary (Cs) capacitance:

$$C_P = \left(\frac{N_S}{N_P}\right)^2 C_S \quad (3)$$

$$= (64)^2 (36 \cdot 10^{-12})$$

$$= 0.15\mu F$$

The majority of the secondary capacitance comes from the series connected lamp and ballast capacitor. The lamp appears as an AC short circuit for much of the cycle, making the equivalent capacitance a little less than the ballast capacitor value. Distributed winding capacitance, stray PC board and lamp wiring capacitance contribute to the small secondary capacitance. Setting the load capacitance equal to the ballast capacitor value is therefore a reasonable initial estimate. Distributed transformer winding and stray capacitance are ignored for initial calculations. Parasitic capacitances have negligible effect on the primary capacitance since its value is several orders of magnitude larger than on the secondary.

With the independent primary and secondary resonant tank frequencies approximately equal, the secondary circuitry is reflected to the primary, allowing treatment as a single resonant tank. With both the primary and secondary resonant tanks set to the same frequency, the equivalent resonant capacitor (Cr) is simply twice Cp. The primary inductance is then calculated to give the desired resonant frequency:

$$L_P = \frac{1}{(2\pi F)^2 C_R} \quad (4)$$

$$= \frac{1}{(2\pi 50 \cdot 10^3)^2 (0.3 \cdot 10^{-6})}$$

$$= 34\mu H$$

Primary and secondary RMS currents are then calculated to determine maximum acceptable transformer winding resistances. The secondary current is mostly lamp current, although the currents to drive distributed winding and stray wiring capacitances are also factors. For now we will ignore these parasitic effects, since in most cases the additional loss they cause will not be enough to significantly alter the transformer design.

Each half of the primary winding sees an asymmetrical sinusoidal current which is the sum of the primary resonant current and the input current source from the buck regulator during one-half of the cycle. The primary voltage must be calculated first in order to determine the primary resonant current:

$$V_P = \frac{N_S}{N_P} V_S \quad (5)$$

$$= \frac{N_P}{N_S} \sqrt{V_{CB}^2 + V_{LAMP}^2}$$

$$= \frac{1}{64} \sqrt{(700)^2 + (350)^2}$$

$$= 12.2V(peak)$$

The primary resonant current is then:

$$I_R = \frac{V_P}{Z_P} \quad (6)$$

$$= \frac{V_P}{\sqrt{\frac{L_P}{C_P}}}$$

$$= \frac{12.2}{\sqrt{\frac{34}{0.15}}}$$

$$= 0.810A(peak)$$

The buck regulator current is calculated by equating input and output power while assuming 90% efficiency for the push-pull stage:

$$P_{IN} = \frac{P_{OUT}}{0.9} \quad (7)$$

$$= \frac{V_{LAMP(RMS)}\, I_{LAMP(RMS)}}{0.9}$$

$$= \frac{(248)(5.55 \cdot 10^{-3})}{0.9}$$

$$= 1.53W$$

The buck regulator sources current to the push-pull stage through the primary winding's centertap. The average voltage at this point is one-half of the total primary voltage. The average buck regulator output voltage is therefore one-half the average primary voltage calculated in (5):

$$V_{BUCK} = \frac{V_P}{\pi} \quad (8)$$

$$= \frac{12.2}{\pi}$$

$$= 3.88V\ (avg)$$

The buck output current is then:

$$I_{BUCK} = \frac{P_{IN}}{V_{BUCK}} \quad (11)$$

$$= \frac{1.53}{3.88}$$

$$= 0.394A$$

During the first half of the resonant cycle, one-half of the primary winding conducts the resonant current, while the other half of the primary winding conducts the sum of the resonant current and the buck regulator current. During the second half of the cycle the conditions reverse such that both halves of the primary conduct the same asymmetrical current 180 degrees out of phase from each other. A close approximation of the primary current is made by simply adding the average value of the buck output current to the peak resonant current for one-half of the cycle, and calculating the rms value as an asymmetrical sinewave:

$$I_{PRI} = \sqrt{\left(\frac{I_R}{2}\right)^2 + \left(\frac{I_R + I_{BUCK}}{2}\right)^2} \quad (12)$$

$$= \sqrt{\left(\frac{0.810}{2}\right)^2 + \left(\frac{0.810 + 0.394}{2}\right)^2}$$

$$= 0.725A(rms)$$

PUSH-PULL TRANSFORMER

All parameters necessary to design the transformer are now known and an initial design can be started. Optimal transformer design for this application is beyond the scope of this paper. The additional complexity of the resonant circuitry, along with the high output voltage and small required size present a significant mechanical design challenge. Any variable can be iterated since the ballast capacitor value was arbitrarily selected. Optimal design normally requires many design iterations.

Often the preceding analysis is done by a transformer manufacturer that specializes in resonant ballast design. A standard transformer from Coiltronics, Inc. [5], which is intended specifically for portable computer LCD back lighting was selected for the design example. Its specifications closely match the application's requirements. Selecting a standard transformer eliminated numerous iterations and reduced the design cycle considerably. The Coiltronics transformer has the following specifications:

CTX110600-1 specifications:

Primary Inductance	44mH
Ns/Np	67
Primary Resistance	0.160 ohms
Secondary Resistance	176 ohms

The CTX110600-1 employs a unique method of secondary winding termination. The secondary return lead terminates at the primary centertap, making it unnecessary to insulate it from the rest of the winding. Distributing the secondary across several sections of a multi-section bobbin also eliminates insulation between winding layers. The secondary current has negligible effect on the primary since its value is roughly two orders of magnitude smaller than the primary current. This connection scheme does add a small amount of asymmetry to the secondary voltage waveform, but again, this effect is negligible.

To design with an existing transformer, the equations are rearranged to calculate the nominal capacitor values, or the capacitor values are recommended by the transformer manufacturer. Some experimentation is usually necessary, regardless of how the initial paper design is done, to achieve the optimum circuit for a particular application.

BUCK REGULATOR

The ZVS push-pull converter's resonant frequency establishes the buck and flyback regulators' conversion frequency. Each time the push-pull converter's primary voltage crosses through zero, the UC3871's oscillator is reset. The design frequency for both the buck and flyback circuits is therefore twice the minimum push-pull resonant frequency.

The buck regulator provides a regulated, variable output voltage for the push-pull converter to reject input voltage variations and allow lamp brightness adjustment. Due to the absence of a large output capacitor, the buck regulator presents a high impedance to the push-pull converter at its resonant frequency. Neglecting the sawtooth ripple, the output inductor's current is nearly constant.

Inductor ripple current is greatest when the duty cycle and frequency are minimum. This occurs at maximum input voltage and lamp current, where the buck OFF time is maximum:

$$T_{OFF(MAX)} = \frac{1-D}{F_{MIN}} \quad (13)$$

$$= \frac{1-D}{F_{MIN}} \left(1- \frac{V_{BUCK}}{V_{IN(MAX)}}\right)$$

$$= \frac{1}{10^5} \left(1- \frac{3.88}{18}\right)$$

$$= 7.84\mu s$$

To minimize inductor value, ripple current is normally 30% to 50% of the average value.

$$L > \frac{T_{OFF}\ V_{BUCK}}{I_{RIPPLE}} \quad (14)$$

$$> \frac{(7.84 \cdot 10^{-6})(3.88)}{(0.5)(0.394}$$

$$> 154\mu H$$

A Coiltronics part number CTX150-4 was selected for the buck inductor that has the following specifications:

Inductance	150µH
Resistance	0.175 ohms
Rated Current	0.72ADC

CONFIGURING THE CONTROL CIRCUITRY OSCILLATOR

The UC3871 contains a synchronizable oscillator internally configured to operate over a 3:1 frequency range. A 200µA current source is used to charge an external capacitor (Ct) from 0.1V to 3.0V. At the 3.0V threshold, a 4.0mA current sink discharges the capacitor back down to 0.1V. The zero detect input senses the transformer primary centertap voltage and indicates when the resonant tank voltage is crossing through zero. Under normal circumstances, the zero detect input will trigger the discharge circuit before the capacitor voltage reaches the 3.0V threshold, synchronizing the oscillator to twice the resonant tank frequency.

To improve noise immunity and prevent false triggering from comparator chatter, another comparator is used to lock out the zero detect input until Ct's voltage reaches 1.0V. The 3V maximum, 1V minimum peak oscillator amplitudes establish a 3:1 synchronization range. Ideally, the synchronization range should be centered around the resonant frequency range. A good starting point is to set the oscillator amplitude (Vct) to 2.2V at the minimum synchronization frequency, which is twice the minimum resonant frequency. The timing capacitor value is then:

$$C_T = \frac{10^{-4}}{F} \quad (15)$$

$$= \frac{10^{-4}}{10^5}$$

$$= 1.0nF$$

The resonant tank frequency must always be within the oscillator synchronization range to prevent severe output distortion and non-ZVS operation.

A 10k resistor in series with the zero detect input is recommended to protect against high voltages that occur during turn-off. The zero detect input is specified to withstand a maximum input current when driven from a high impedance source. A capacitor connected to the transformer center-tap limits the maximum voltage at turn-off by absorbing all of the inductive energy in the buck inductor when both of the push-pull MOSFETs turn off. This capacitor also attenuates noise and ringing which would otherwise be present at this node.

SOFT-START AND OPEN LAMP DETECT

The primary function of soft-start is to allow time for the lamp to strike and conduct the programmed level of current before enabling the open lamp detection circuitry. A 20µA current source charges an external capacitor (Css) when either the supply voltage exceeds the nominal 4.2V under-voltage lockout, or the IC is enabled. Once the external capacitor voltage exceeds 3.4V, the open lamp detect circuit is enabled. The soft-start time is normally determined empirically, since many factors such as minimum supply voltage and temperature influence the time it takes the lamp to strike. A 150ms soft-start was required to insure that the lamp started in the application example circuit. Once the soft-start time is determined, the capacitor value is calculated by:

$$C_{SS} = 5.9 \cdot 10^{-6}\ T_{SS} \quad (16)$$

$$= (5.9 \cdot 10^{-6})(0.15)$$

$$= 0.88\mu F \text{ (use} = 1\mu F)$$

An open lamp is detected by sensing that the current feedback loop has opened. During normal operation the current loop is closed, and the error amplifier inverting input is at 1.5V. If the lamp circuit either opens or shorts to ground, insufficient feedback voltage develops, and the inverting input voltage drops to a level determined by input offset current and radiated signal pickup. Input bias current limits the maximum feedback resistor value to 100k, with lower values providing greater margin at

the expense of requiring a larger compensation capacitor. Radiated signal pickup is a more complex problem, and is addressed later in the PC board layout considerations section.

LAMP CURRENT CONTROL LOOP

The UC3871 controls lamp intensity by closing an average current feedback loop around the buck regulator and push-pull resonant converter. Optimal compensation of this system is extremely difficult because of the complex output stage and load characteristics. High frequency response is dominated by a resonant double pole formed by the buck inductor and primary resonant and load capacitances reflected to the transformer center-tap. Typically, this double pole has a Q between 1 and 5, and occurs less than a decade below the resonant tank frequency unless an excessively large value is used for the buck inductor. Furthermore, the current feedback signal must be filtered sufficiently for correct PWM operation, requiring significant signal attenuation at the resonant tank frequency. These factors make it nearly impossible to cross the loop over above the output stage's double pole.

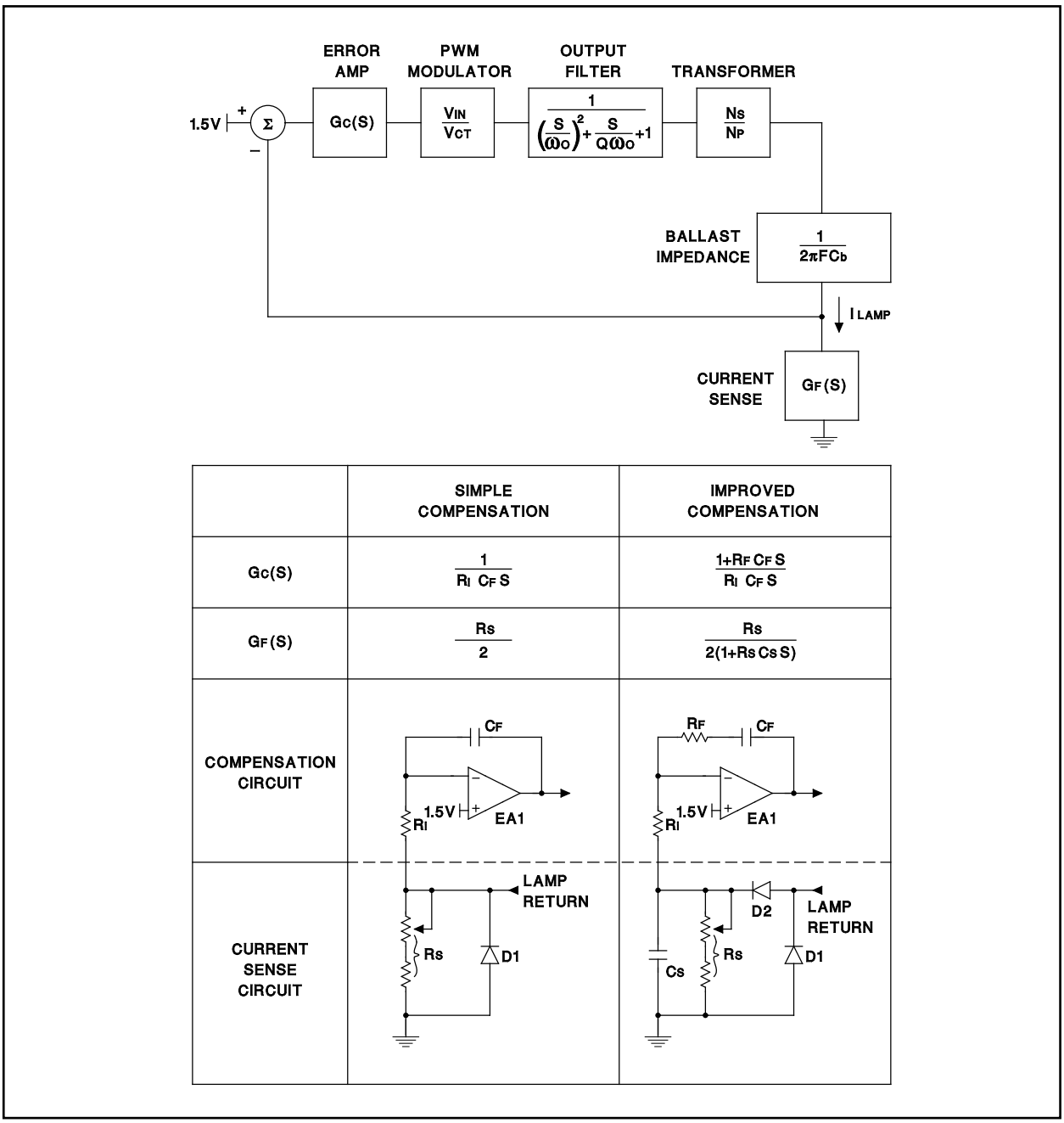

Figure 3. Control loop block diagram.

Below the double pole the power stage gain is flat. The simplest way to compensate the loop is to introduce a low frequency dominant pole that sets the unity gain crossover frequency well before the output filter double pole. This pole also sufficiently filters the half-wave rectified current feedback signal for proper PWM operation. The design example circuit shown in figure 2 employs this compensation technique, which requires a minimal number of components. Figure 3 shows the circuit's control loop block diagram. With the unity gain frequency set well below the resonant double pole, higher frequency effects caused by capacitor ESR and transformer leakage inductance can be ignored.

Three of the blocks exhibit gain variation with input or load changes. Most notable is the current sensing resistor, which in a typical application will cause a 25dB to 30dB gain change over the lamp current adjustment range. The ballast capacitor (Cb) is treated as a fixed impedance determined by the converter's resonant frequency, but since the resonant frequency varies about 20% in an actual application, the ballast impedance varies inversely by the same amount. The modulator gain is directly proportional to frequency since the PWM ramp amplitude (Vct) varies inversely with frequency, and to a first order, cancels the ballast impedance variation. The more dominant modulator gain variation however, is from the input supply voltage (Vin), which may vary more than 3:1.

The output filter resonant frequency is determined by the buck inductor value and the equivalent value of the primary resonant, output ballast, and output stray capacitances reflected to the buck regulator output:

$$\omega_O = \sqrt{L_{BUCK}\, C_{EQ}} \qquad (17)$$

$$C_{EQ} \approx 4C_P + \left(\frac{N_S}{N_P}\right)^2 C_B$$

$$\approx 8C_P$$

Output filter Q is the ratio of the resonant tank impedance to the effective series damping resistance:

$$Q = \frac{\omega_O L}{R_{SERIES}} \qquad (18)$$

The effective series resistance is the sum of all power circuit resistances reflected to the buck regulator output, plus the reflected load resistance transformed to its effective series value (Rseries). With every effort made to minimize series resistance for maximum efficiency, the reflected load term dominates.

$$R_{SERIES} \approx \frac{V_{BUCK}^2}{1.1\, P_{OUT}} \text{ (ohms)} \qquad (19)$$

Output filter Q is greatest at minimum lamp current. Gain peaking at the filter resonant frequency is then:

$$G_{PEAK} = 20 \log Q_{MAX} \text{ (dB)} \qquad (20)$$

The maximum unity gain crossover frequency is typically set nearly a decade below the output filter resonant frequency to insure adequate gain margin. Loop gain (and crossover frequency) is greatest at maximum input voltage and minimum current. At minimum input voltage and maximum lamp current, the unity gain crossover frequency may decrease two decades or more. Fortunately, wide bandwidth and good transient response are not required in most applications.

The example circuit's output filter has a maximum Q of 3, and a resonant frequency of 13kHz. The maximum unity gain crossover frequency is 1.5kHz, giving a worst case gain margin of about 9dB.

IMPROVED LOOP COMPENSATION CIRCUIT

Some applications require quick transient response to prevent lamp flicker from input voltage disturbances. Systems which have poor input supply regulation, particularly those with transient loads or a pulsed current battery charger are examples of such applications. With the typical UC3871 circuit, lamp current is adjusted by varying the closed loop gain. This causes the unity gain crossover frequency to decrease one decade for each 20dB increase in lamp current.

The control loop block diagram in figure 3 shows an improved current sense and loop compensation scheme that makes the unity gain crossover frequency insensitive to lamp current adjustment. A capacitor (Cs) connected in parallel with the current sense resistor forms a pole that varies directly with the current sense gain. This configuration provides variable low frequency gain for lamp current adjustment with fixed high frequency gain for constant loop crossover frequency.

This pole can theoretically provide acceptable loop compensation with a fixed error amplifier gain, but the required value for Cs would be much to large for a practical circuit. Adding a pole-zero pair to the error amplifier allows for an acceptable Cs value and provides high DC gain by maintaining a pole at the origin. The current sense pole (1/(RsCs)) and

the error amplifier zero (1/(RfCf)) are placed at the control loop's unity gain crossover frequency with Rs set to its minimum value.

LCD BIAS SUPPLY FLYBACK REGULATOR

The design procedure for the flyback converter is not given here since it differs little from a conventional power supply application. The only unique condition is that the conversion frequency varies with the push-pull converter's frequency. As with the buck converter, the initial design frequency is twice the minimum resonant frequency (the design example's buck and flyback regulator's minimum frequency is 100kHz). At the lowest lamp brightness, the frequency will typically increase 15% to 25%, minimally influencing the flyback converter's operation.

For the design example, the flyback converter is operated in the continuous inductor current mode. For most power supply applications, this mode of operation is avoided because of the poor closed loop bandwidth dictated by the right-half plane zero in the transfer function. Continuous mode operation does result in lower power stage loss however, and since for this application power loss is usually more critical than dynamic response, it is normally the preferred mode of operation.

The minimum component compensation circuit shown in the design example schematic employs a dominant pole to cross over the loop before the output stage's resonant double pole. Output voltage overshoot at power-up can be significant with this configuration if the error amplifier's integration capacitor is allowed to fully charge as the output voltage slews to its nominal value. This large signal problem is exacerbated by the ground referenced error amplifier configuration, which only allows a small discharge current to be developed.

For the design example, a 0.1µF integration capacitor is used although a value nearly ten times smaller will provide maximum loop bandwidth. The 0.1µF capacitor charges slowly during power-up, and eliminates overshoot by soft-starting the supply. A shottky diode (BAT81) is used to clamp the non-inverting error amplifier input to prevent it from phase inverting and latching up the control loop. This diode should have a forward drop less than 0.5V at room temperature.

IMPROVED FLYBACK COMPENSATION

As with the lamp driver circuit, there are applications that require better transient response than is achievable with dominant pole compensation. A simple alternative technique, shown in figure 4, is to cancel one of the output stage's resonant poles by a zero in the compensation circuitry, and cross the loop over at about 1/4 the minimum right-half plane zero frequency. This technique does result in lower DC gain than the dominant pole circuit used in the design example, but offers much better large signal behavior and a decade or more increase in loop bandwidth. Another pole-zero pair can be added to improve DC load regulation and input line rejection, although this additional complexity appears unnecessary.

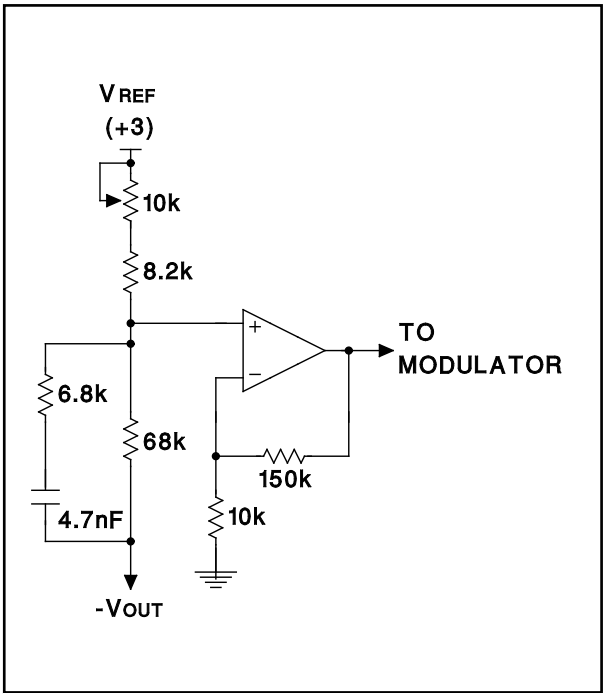

Figure 4. Improved flyback regulator compensation.

Discontinuous inductor current operation is also an option to significantly improve transient response if a small decrease in efficiency is tolerable. Discontinuous mode compensation is illustrated in the following positive output, coupled inductor flyback circuit.

POSITIVE OUTPUT VOLTAGE FLYBACK REGULATOR

A positive output LCD bias supply circuit is more complicated than the negative output, because the output voltage can be greater or less than the input voltage. This eliminates both buck and boost circuits, and makes the coupled inductor flyback converter a good choice for this application. Discontinuous inductor current operation is employed in the circuit shown in figure 5, allowing simple compensation and excellent transient response.

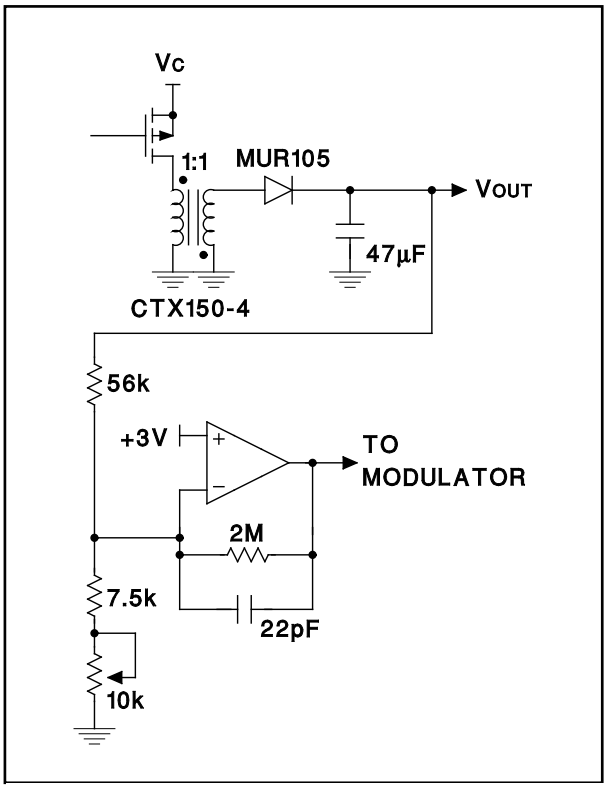

Figure 5. Positive output coupled inductor flyback regulator.

Since the output MOSFET is relatively large, and has significant output capacitance and avalanche energy capability compared to the current it must switch, a clamp or snubber network is not required to insure reliable operation. Snubbing may be necessary to reduce EMI however. This circuit can, of course be operated with continuous inductor current for a small improvement in efficiency. The compensation circuitry would then be similar to the previous flyback regulator examples. Flyback regulator and control loop design is covered in the references.

PRACTICAL CONSIDERATIONS

MEASUREMENT TECHNIQUES

The combination of low power, high voltage, and high frequency AC present a unique challenge in determining circuit efficiency. An absolute efficiency measurement is important because it allows meaningful comparison with work done by others. Since an electrical efficiency measurement removes lamp performance from the equation, it is the most universal performance index.

For an actual application however, high output light intensity for a given input power is the actual design goal. Once reasonable electrical efficiency is achieved, further circuit refinement should be based on relative light intensity efficiency improvements using the same lamp and test setup.

To measure electrical efficiency, extreme attention to measurement technique and equipment is required. Output current is relatively easy to measure with a current sense resistor in series with the lamp return to ground. For the design example circuit shown in figure 2, a small resistor can be added in series with R5 and D2 to measure both half cycles of the lamp current.

To measure lamp voltage, a 100X or 1000x oscilloscope probe with low input capacitance and good high frequency accuracy is required. Accurate AC probe calibration is critical in achieving a meaningful measurement. At low lamp current, both the lamp current and voltage exhibit clean sinusoidal waveforms with minimal harmonic distortion. The product of the RMS lamp current and voltage then give an accurate measurement of the output power. As current is increased, the lamp's nonlinearity becomes apparent, as significant distortion is observable in the lamp voltage waveform. The product of the RMS lamp current and voltage will no longer yield an accurate output power measurement.

A true RMS measurement that is insensitive to waveform shape is made by taking the average product of the instantaneous lamp voltage and current. Many digital oscilloscopes provide this function with reasonable accuracy. The accuracy of this technique can be further improved by calibrating to a known sinusoidal source.

EFFICIENCY OPTIMIZATION

Most of power lost in the lamp driver circuit is dissipated in the transformer, inductor, MOSFETs, primary resonant capacitor, buck regulator diode, and the UC3871. Although the output ballast capacitor (Cb) dissipates little power, its value greatly influences the performance of the circuit. Consider the effect of increasing Cb such that the secondary voltage drops 10%. The transformer's flux density and primary resonant current decrease 10%, reducing both transformer core and winding losses. Both of these losses are exponential, so the power savings can be significant. Smaller transformer losses decrease the input power required, reducing the current through, and the power lost in the other power handling components.

Of course the ballast capacitor cannot be continually increased, as waveform distortion will quickly become unacceptable, but there is an optimal value for a particular application that is best deter-

mined experimentally. The same is true for the primary resonant capacitor, where a decrease in value will increase the resonant frequency, and decrease the resonant current and associated losses. Again, there is an optimal value that yields the best distortion/efficiency tradeoff for a particular application.

The losses contributed by the other power components are more easily determined, as circuit operation is affected minimally by their variation. For lowest loss, MOSFETs are selected for minimal combined conduction and gate drive loss. Bigger is not necessarily better! Logic-level threshold devices are required for high efficiency at low input supply voltages, although standard threshold devices will usually function with reduced efficiency down to about 6V.

The primary resonant capacitor, Cp conducts the primary resonant current and must have low losses for good circuit efficiency. A monolithic ceramic capacitor, and several film capacitors from Electronic Components, Inc. [6], were evaluated to determine the relative performance differences among various dielectric and construction techniques. Polypropylene film/foil capacitors exhibit the lowest losses. Metalized polypropylene capacitors are usually smaller than foil/film construction, but will result in about a 1 percent decrease in efficiency.

Further size reduction is possible with polycarbonate or polyester capacitors, but efficiency will be about 1 percent to 3 percent lower than the foil/film polypropylene units. Since the capacitor value is too high for an NPO dielectric, ceramic capacitors must be avoided. The dissipation factor of Z5U and X7R ceramics is much too high for reasonable efficiency. A Z5U monolithic ceramic reduced efficiency more than 12% in the test circuit!

Separate bias (Vcc) and collector (Vc) supply inputs are provided by the UC3871 to take advantage of its ability to operate down to 4.5V. Supplying Vcc from a switching regulated supply while operating the rest of the circuit directly from the battery typically saves from 30mW to more than 100mW.

The buck inductor's winding resistance will dissipate significant power if its winding resistance is excessive. Minimum inductor values are therefore usually preferred to maintain reasonable size. This results in high ripple current that can lead to high core loss. Like all the other power components, every source of dissipation must be investigated and analyzed to squeeze maximum efficiency from the converter.

PC BOARD LAYOUT CONSIDERATIONS

As with all switching regulators, PC board layout is critical. The circuitry should be as compact as practical, particularly in the power stage areas that conduct pulsed current or high voltage. EMI generated by high di/dt is minimized by keeping the pulsed current loops as small as possible. For example, the buck regulator MOSFET and rectifier should be as close together as possible. A low impedance bypass capacitor (a 6.8µF tantalum was used in the application circuit) should also be connected directly between the MOSFET source and the rectifier anode.

The lamp's high operating voltage, and poorly shielded leads and terminals are a potential source of radiated EMI. A significant benefit of the sinusoidal voltages and currents inherent to a fully resonant power stage is the comparatively low voltage and current slew rates. Some high frequency harmonics are present due to distortion and conducted noise received from the buck and flyback regulator power stages, although these are normally very small.

Shielding is normally an effective technique for attenuating EMI generated by high dv/dt nodes, but the performance tradeoffs with the high voltage ballast circuity can be misleading. Shields (or ground planes) increase the capacitive loading on the circuit, but the shield itself dissipates negligible power. When a shield is added however, circuit efficiency will drop because the additional load capacitance will increase the resonant current, just as if the primary resonant capacitance were increased. This effect is minimized by making high voltage traces as short as possible.

Loss due to leakage current in the high voltage section is also possible, particularly as the assembly ages and the PC board surface becomes contaminated. Milling slots in the PC board is a good way to get sufficient creapage distance between the high voltage traces and the rest of the circuitry while maintaining a compact layout.

Another important consideration in the high voltage area is the length and routing of the return lead and PCB trace connecting to the current sense circuitry. If a fault opens the lamp circuit, the error amplifier will command maximum secondary voltage in an attempt to keep the current loop closed. The stray capacitance between the high voltage circuitry and the return lead may conduct sufficient current to keep the loop closed, particularly at low command current and maximum input voltage. This condition will prevent open lamp detection and severely over stress the circuitry.

This problem is avoided by keeping the lamp return path as short as possible, with the current sense resistor placed as close to the lamp as practical. Traces between the current sense resistor and the UC3871 are insensitive to noise and switching harmonics since the signal is DC at this point. Ideally, the majority of the return path length is placed between the current sense resistor and the feedback resistor.

Keeping the high voltage path as short as possible helps by reducing the radiated signal. Shielding around the high voltage area also reduces the radiated signal, but may not be practical in many application. The dimming range should be set no wider than necessary since high current sense resistor values increase sensitivity to this problem. The circuit described in the following section for wide dimming range applications is significantly more robust in this regard, and should be considered when packaging constraints force non-ideal layout.

WIDE DIMMING RANGE APPLICATIONS

Most cold cathode fluorescent lamps function acceptably down to about 1/20 of their rated current. Below this level, they begin to illuminate unevenly across the tube. This “thermometer” effect is caused by parasitic capacitive current, and is heavily influenced by shielding and grounding. Wide dimming ranges are accommodated without uneven lamp brightness by driving the lamp at maximum current, and pulse width modulating the current on and off at low frequency.

Figure 6 shows modifications to the standard application circuit for low frequency PWM control. A fixed current sensing resistor sets the maximum lamp current. An external PWM signal drives the inverting error amplifier input through a series diode and resistor. The input resistor value is chosen to force the lamp current to zero when the PWM input is pulled high. These modifications

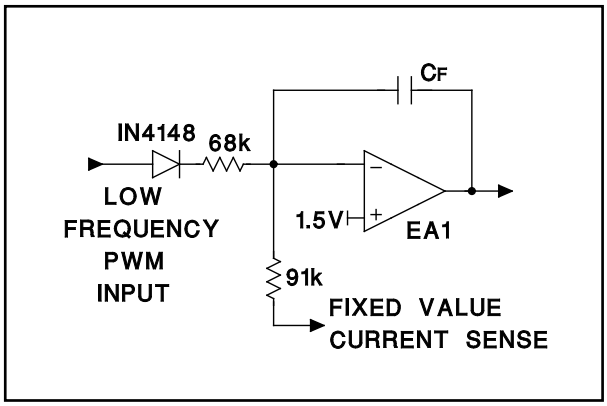

Figure 6. Low frequency PWM control for wide dimming range aplications.

where made to accept a 100Hz PWM signal from 5V CMOS logic through a 1N4148 and a 68k resistor. A 680 ohm current sense resistor set the continuous lamp current at approximately its rated value. Fixed current gain allowed the compensation capacitor (Cf) to be reduced to 4.7nF for more optimum loop performance.

With no further modifications, the circuit maintained uniform lamp intensity over a current range of more than a 500:1. Operation was linear with negligible effect from input voltage variation, down to about 1% of rated current. Below 1%, the current rise and fall time became significant, limiting the practical open loop dimming range to about 100:1. An accurate, stable dimming range greater than

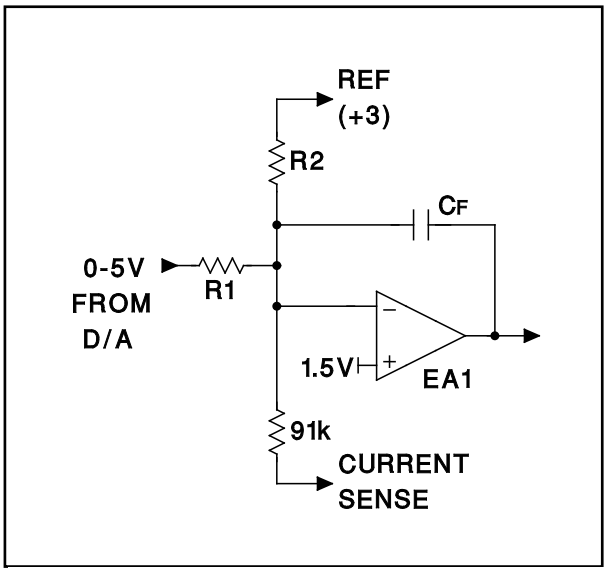

Figure 7. External voltage command interface.

500:1 can be achieved with the addition of a low bandwidth outer current or lamp intensity feedback loop.

DIGITAL LAMP CURRENT CONTROL

The preceding technique for wide dimming range applications is also the best method for digital lamp intensity control. A 100Hz PWM signal generated by a microprocessor combines excellent dimming range with single line digital control. An alternative approach is to use the circuit shown in figure 7, where a D/A injects a command signal into the control loop. This technique provides excellent performance for less than 20:1 dimming ranges, but unfortunately it also defeats the open lamp detect circuit. A third approach is to replace the current sense potentiometer with a digital pot or a multiplying D/A converter, but these devices can usually only handle low current.

BIPOLAR TRANSISTOR OUTPUT STAGES

When cost is more critical than performance, PNP bipolar transistors can be substituted for the P-channel MOSFETs. High gain, low saturation devices such as the Zetex [7] ZTX788B (3A, 20V PNP) perform quite well for the buck regulator when the input voltage is low. A PNP can also be used for the flyback converter, but at a greater efficiency reduction than the buck regulator because it requires a higher voltage device and has greater switching losses.

Simple high speed base drive is implemented by choosing a base resistor for sufficient drive at the minimum input voltage. A small capacitor in parallel with the base resistor improves switching speed. Bipolar NPNs in place of the N-channel MOSFETs are generally a poor cost/performance tradeoff, but can be used if performance is secondary.

CIRCUIT DISABLE

The UC3871 provides an enable input to shut down both converter power stages and put the control circuitry in a very low current standby mode. Applications that require disabling each converter independently require a different approach. The flyback section can be disabled by either pulling the current sensing input above its 0.5V threshold, or by pulling the inverting error amp input above Vref to force the duty cycle to zero.

The ballast converter is a little more difficult to disable because of the open lamp detect circuitry. Any technique that breaks the feedback loop, such as grounding the error amp output, will cause the converter to latch off. Grounding the soft-start input will not bring the duty cycle zero, and therefore will not completely disable the converter. The best shut down method is to source enough current into the inverting error amp input to force its output to ground. This saturates the loop, causing the duty cycle to go to zero without falsely indicating an open lamp condition.

MULTIPLE LAMP CIRCUITS

The ballast circuit is easily modified to drive two or more parallel lamps by splitting the ballast capacitance into two or more capacitors of equivalent value. Because of lamp mismatch, the dimming range must normally be less than single lamp circuits. Additionally, a higher ballast capacitor voltage than is optimum for a single lamp may be required to insure that both lamps start.

DESIGN EXAMPLE PERFORMANCE AND WAVEFORMS

Figures 8 through 10 show typical ballast waveforms from the design example (figure 2) delivering 1.0W into a lamp from a 10V input supply. Figure 8 shows the primary voltage waveforms. Note that the center-tap waveform is one-half the amplitude of the push-pull waveforms, and that no distortion or ringing is evident at the cusps of the waveform.

Figure 9 shows the primary current waveforms and the differentially sensed transformer primary voltage waveforms. The transient steps at the peaks of the primary current are from the push-pull switches turning on, which allow input (reflected load) current to conduct in addition to the resonant current.

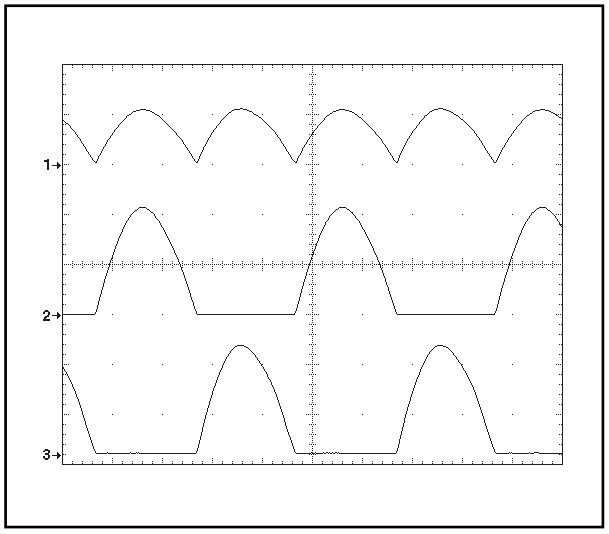

Figure 8. 1. Centertap voltage 5V/div
2. Q1 drain voltage 5V/div
3. Q2 drain voltage 5V/div
Horizontal: 5µs/div

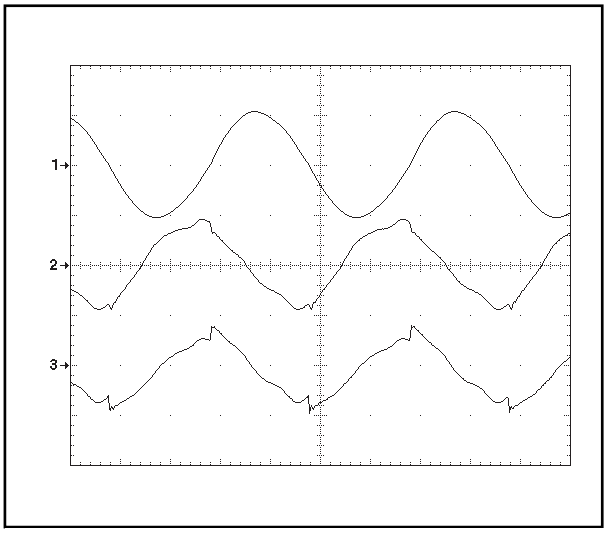

Figure 9. 1. Differential primary voltage 10V/div
2. Primary resonant capacitor current 0.5A/div
3. Primary transformer winding current 0.5A/div
Horizontal: 5µs/div

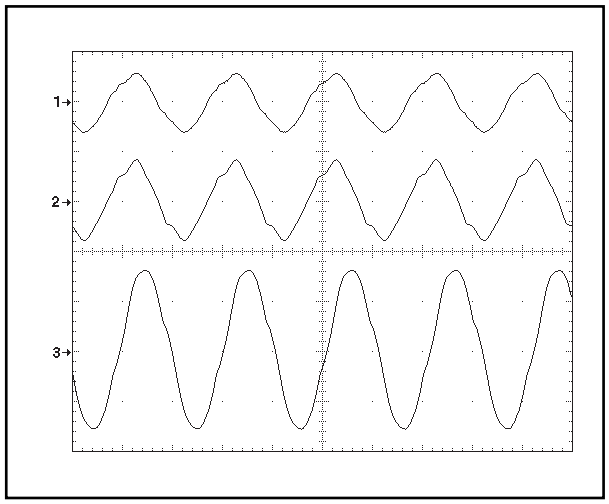

Figure 10. 1. Lamp current 10mA/div
2. Lamp voltage 500V/div
3. Transformer secondary voltage 500V/div
4. Horizontal: 10µs/div

Figure 10 shows the secondary voltage and current waveforms. Lamp current and voltage are in phase indicating that the lamp appears resistive. These waveforms lead the secondary voltage waveform because of the capacitive coupling. Distortion in the lamp voltage waveform is caused by lamp impedance nonlinearity, which also causes some distortion in the secondary voltage waveform.

Figures 11 and 12 illustrate circuit efficiency with varying input supply voltage and output power. In both cases a separate 5V supply powered Vcc, since this is available in most applications. Figure 11 shows the efficiency of the complete converter over an input supply range of 5.5V to 18V. For this plot, the lamp power was 1.0W, and the LCD bias power was 0.324W (18V across 1k). The sudden decrease in efficiency at low input voltage is from insufficient gate drive voltage. This efficiency drop can be eliminated by using logic level MOSFETs.

The efficiency curve in figure 12 was taken with the flyback converter output disabled, although the control circuitry was still active. The lamp power was then varied from 0.2W to 1.9W while keeping the supply voltage at 10V. Above about 3/4W, efficiency was greater than 80%. At light load, the control circuit and gate drive losses became significant, and efficiency was greatly reduced.

SUMMARY

The UC3871 provides a complete power supply control solution for backlit LCDs. A design method illustrated with a circuit example has been presented, along with alternate configurations and loop compensation techniques. Example circuit waveforms and efficiency graphs show that the UC3871 provides a simple, yet high performance solution.

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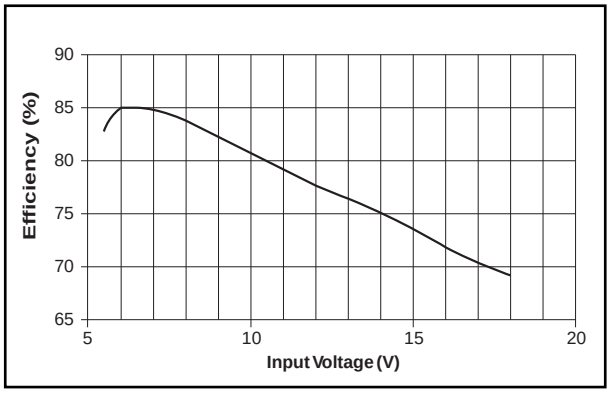

Figure 11. Efficiency vs. input voltage for 1.324W output.

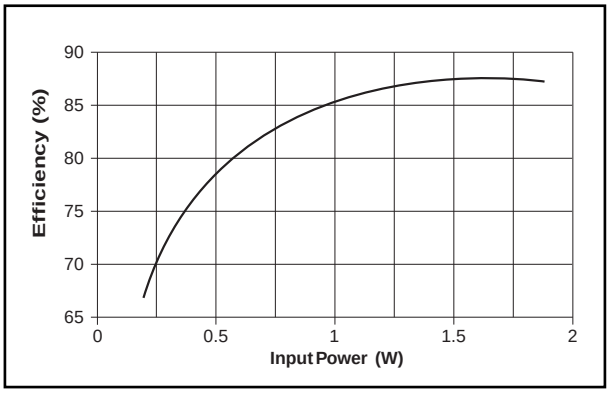

Figure 12. Efficiency vs. output power for 10V input.

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